REMARKS

Claims 1-20 are currently pending. In the May 16, 2007 Office Action, the Examiner objected to claim 7 for an informality; rejected claims 1-3, 6, 8-10, 12-15, 17, 18 and 20 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 7,099,325 to Kaniz et al. ("Kaniz"), and rejected claim 7 under 35 U.S.C. § 103(a) as being unpatentable over Kaniz in view of U.S. Patent Publication No. 20040122973 to Keck et al. ("Keck"). The Examiner indicated that claims 4, 5, 11, 16, and 19 would be allowable if rewritten in independent form. While Applicants appreciate the Examiner's indication of allowable subject matter and reserve the right to amend the claims as suggested by the Examiner, Applicants respectfully traverse the rejections for the reasons set forth hereinbelow.

A. Claim 7 Has Been Amended To Overcome The Objection

In response to the Examiner's objection to the noted informality of claim 7, Applicants have amended the claim to spell out "HyperTransport" as suggested by the Examiner, and therefore request that the objection be withdrawn.

B. Claims 1-3, 6, 8-10, 12-15, 17, 18 and 20 Are Not Anticipated by Kaniz

In response to the Examiner's rejection of claims 1-3, 6, 8-10, 12-15, 17, 18 and 20 as being anticipated by Kaniz, Applicants respectfully request reconsideration and withdrawal of the rejection because Kaniz's disclosure of a multiport switch (which selectively forwards received data packets to one or more transmit ports) does not anticipate the present invention's "multiprocessor switching chip" which uses a routing circuit to select one of "plurality of destination modules within the multiprocessor switching chip" for a received packet. *See, e.g.*, claims 1 and 6 ("the routing signal is encoded in the form of an output virtual channel that is used by the multiprocessor switching chip to route packets to destination modules on the multiprocessor switching chip") (emphasis added). Nor does Kaniz disclose "routing a packet to one of a plurality of destinations in a processor circuit," as recited in claim 14. Finally, Kaniz entirely fails to disclose any notion of using extracted "input virtual channel information" to generate "an output virtual channel" in the course of routing packet data, as recited in claim 20.

At best, Kaniz discloses "a multiport switch 180" which uses lookup tables to forward received data packets to one or more transmit ports. *See* Kaniz Patent, Fig. 3 and col. 7, lines 16-

34 ("As shown in FIG. 3, a frame is received on receive port 302 and transmitted from ports 311 and 314."). In this respect, the multiport switch disclosed in Kaniz is simply performing a packet switching function in a packet switched network. *See* Kaniz Patent, col. 1, lines 18-19 ("The present invention relates generally to switches in a packet switched network…."). However, there are numerous aspects of the claimed invention that are wholly missing from the Kaniz disclosure.

As a preliminary matter, the disclosed multiport switch from Kaniz does not meet the "multiprocessor switching chip" requirement recited in claims 1-13. Nor does Kaniz disclose a routing circuit that is configured to route a received packet by selecting a received packets to a destination module "within the multiprocessor switching chip," all as recited in claims 1-13. On this point, Applicants have carefully reviewed the cited Kaniz passages relied upon by the Examiner (Figure 3, receiver ports 301-304, transmission ports 311-314; col. 6, lines 9-22, lines 36-38 and lines 46-51; and col. 7, lines 21-22, lines 29-32 and lines 61-64), and there is simply no teaching or suggestion of a "multiprocessor switching chip," much less "a plurality of destination modules within the multiprocessor switching chip" to which packets are routed by the routing circuit.

Applicants have also reviewed the cited Kaniz passages relied upon by the Examiner to reject claim 3 (Figure 3, external memory 170; col. 5, lines 55-57 and col. 6, lines 42-45), but these passages describe the use of a frame pointer to external memory 170 which stores "data frames" that require transmission, and there is simply no teaching or suggestion in Kaniz that the external memory 170 is a "routing table to output a routing result," much less that the routing result output from the routing table is used to "switch the received packet to a destination module identified by the routing result." On this point, Kaniz explicitly states that the external memory 170 stores data packets, not header information:

> To conserver memory on switch 180, the multiport switch splits the header portion from the data-portion. The data portion may then be stored, by external memory interface 265, off-chip in external memory 170. The header is forwarded to IRC 245. Based on the information in the header, IRC 245 determines, using an address lookup table, the correct transmit port(s) 210 from which the frame is to be transmitted from.

Kaniz Patent, col. 7, lines 20-24 (emphasis added). As seen from the foregoing, Kaniz's external memory 170 is not a routing table that outputs a routing result, as recited in claim 3. Applicants would also note that the requirements of originally-filed claim 6 – which recited routing packets "to destination modules on the multiprocessor switching chip" – are not met by the cited Kaniz disclosure at col. 6, lines 42-45, which states that "The PVQ 235 may decode the forwarding descriptor to obtain the frame pointer. The PVQ 235 may then supply the frame pointer to the appropriate output queues within the output control queues 240." Indeed, the referenced "output control queues 240" are shown in Figure 2 as being connected directly to the transmitter 210, confirming that the routing function of Kaniz's multiport switch is to selectively forward received packets, not to route packets to destination modules in the multiprocessor switch. Based on at least these missing limitations, claims 1-13 are not anticipated by Kaniz.

In addition, the disclosed multiport switch from Kaniz does not meet the requirement of "routing a packet to one of a plurality of destinations in a processor circuit," as recited in claims 14-19. Nor does Kaniz disclose "transferring the first packet to a destination in the processor circuit identified by the routing result," all as recited in claims 14-19. To the extent that the rejection analysis of claim 14 relies on the Kaniz passages (col. 6, lines 9-11 and lines 36-37; and col. 7, lines 21-22 and lines 29-32), Applicants respectfully submit that the cited passages in no way suggest routing packets to destinations in the processor circuit by "transferring the first packet to a destination in the processor circuit identified by the routing result." Again, this flows from the fact that the multiport switch disclosed in Kaniz is simply performing a packet switching function a packet switched network, and as a result, Kaniz is not concerned with routing packets to destinations within the multiport switch 180. The same deficiency in the Kaniz disclosure applies to claim 17, which specifies that the "routing result directly identifies the destination in the processor circuit for the first packet." Applicants would also note that the requirements of claim 18 -- relating to a routing table that output a routing result – are not met by Kaniz's external memory 170 as argued by the Examiner, since Kaniz clearly states that the external memory 170 is used to store the data portions of received packets, and does not store routing results. Based on at least these missing limitations, claims 14-19 are not anticipated by Kaniz.

Finally, the disclosed multiport switch from Kaniz does not meet the requirement of "routing packet data extracted from a packet received on an input virtual channel to an output virtual channel," as recited in claim 20. Indeed, Applicants have carefully reviewed the cited Kaniz passages relied upon by the Examiner (Figure 3, receiver ports 301-304, transmission ports 311-314; Figure 4, source address field 401, destination address field 402; col. 5, lines 55-

57; col. 6, lines 9-22, lines 36-38 and lines 42-51; and col. 7, lines 21-22 and lines 61-64), but there is no reference at all to any "virtual channel," much less routing packet data "received on an input virtual channel to an output virtual channel." In view of the failure to disclose "virtual channel" routing, Kaniz also does meet the requirements of claim 6. Based on at least these missing limitations, claims 6 and 20 are not anticipated by Kaniz.

In view of Kaniz's failure to meet the various requirements of the claimed invention such as recited above, Applicants respectfully submit that the Examiner has incorrectly applied the legal requirements for establishing anticipation by the Kaniz reference. To establish a *prima facie* case of anticipation, the Examiner has the burden of pointing out where each and every element of the claimed invention, arranged as required by the claims, are found in the Kaniz reference, either expressly or under the principles of inherency. *See generally*, In re King, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986); Lindemann Maschinenfabrik GMBH v. American Hoist and Derrick, 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984). This the Examiner has not done. At best, the cited passages from Kaniz disclose a multiport switch for selectively forwarding received packets, but in no way disclose or suggest Applicant's invention of a multiprocessor switch for routing packets to destinations within the multiprocessor switch, such as by routing packet data extracted from a packet received on an input virtual channel to an output virtual channel. Because a *prima facie* case has not been established that the Kaniz meets or suggests the requirements of the claims, Applicants respectfully request that the anticipation rejection of claims 1-3, 6, 8-10, 12-15, 17, 18 and 20 be withdrawn and that the claims be allowed.

C. **Claim 7 Is Not Obvious Over Kaniz in view of Keck**

In response to the Examiner's rejections of claim 7, Applicants respectfully request reconsideration and withdrawal of this rejection. Putting aside for the moment the propriety of combining the Kaniz and Keck references or whether these references even qualify as prior art,[1] there are numerous requirements of the claim are not disclosed by the proposed combination.

Firstly, contrary to the Examiner's assertion that Kaniz discloses all of the limitations of the base claim, Applicants have explained above that Kaniz does not disclose the base claim requirements from claim 1 of a "multiprocessor switching chip" with a "routing circuit" that is configured to route a received packet by selecting a received packets to a destination module "within the multiprocessor switching chip." Nor, as explained above, does Kaniz disclose the base claim requirements from claim 3 of a "routing table to output a routing result to switch the received packet to a destination module identified by the routing result."

As for the specific requirements recited in claim 7, the Examiner concedes that Kaniz "fails to disclose a switch hop route signal that is used to route the received packet over an HT switch device coupled to the multiprocessor switching chip," but asserts that Keck remedies this deficiency with its disclosure of "using hyper transport (HT) link to couple processors and peripheral devices," citing Keck paragraph 4, lines 1-3. The cited passage is set forth below:

> Generally, in multiprocessor computer systems, individual processors and peripheral devices are coupled via Hyper Transport (HT) technology input/output links.

As seen from the quoted passage, there is simply no teaching or suggestion in Keck of a routing table that outputs a routing result in the form of "a switch hop routing signal that is used to route the received packet over an HT switch device coupled to the multiprocessor switching chip." At best, the Keck passage states that processors and peripheral devices are coupled by HT I/O links, but there is no specific mention of how this is done, much less that switch hop route signal is output from a routing table and used to route a received packet, as recited in claim 7.

To establish a *prima facie* case of obviousness, the Examiner has the burden of showing that all the claim limitations are taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974); In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). Having shown that the cited references, individually or in combination, fail to disclose or suggest the invention recited in claim 7, Applicants respectfully submit that a *prima facie* case of obviousness has not been established, and therefore need not address the deficiencies in the Examiner's proposed "motivation to combine" evidence. Alza Corp. v. Mylan Labs., Inc., No. 06-1019 (Fed. Cir. Sept. 6, 2006) (The motivation-to-combine inquiry "prevent[s] statutorily proscribed hindsight reasoning when determining the obviousness of an invention."). Accordingly, Applicants respectfully request that the obviousness rejection of claim 7 be withdrawn and that the claim be allowed.

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[1] In response to the Examiner's assertion of the § 102(e) references, Applicants reserve the right to demonstrate prior conception and reduction to practice.

CONCLUSION

In view of the remarks set forth herein, Applicants respectfully submit that all pending claims are in condition for allowance and request that a Notice of Allowance be issued. Nonetheless, should any issues remain that might be subject to resolution through a telephone interview, the Examiner is requested to telephone the undersigned at 512-338-9100.

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Respectfully submitted,

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